## REMARKS

Claims 19-26 are allowed. The Applicants appreciate the indication of allowability.

Claims 1-2 were rejected under 35 U.S.C. 102 as being clearly anticipated by Beebe et al. (US Patent 6,021,513). Claims 3-18 were rejected under 35 U.S.C. 103 as being unpatentable over Beebe et al. in view of Crouch et al. (US Patent 5,592,493). The Applicants note that Crouch et al. filed their application after the present application was filed and, as such, cannot be used as prior art unless there is a priority claim to a filing prior to invention by the applicants herein which prior filing teaches the claimed invention of the present application. The Applicants do not see a reference on the cover page of Crouch et al. indicating such a priority claim. As such, the Applicants object to the use of Crouch et al. as a secondary reference for the purpose of forming a rejection.

Generally, Beebe et al. teach using a boundary scan chain to test an FPGA. Each of the rejected independent claims has been amended. The original claim language included language that arguably is not taught by the cited art in the present Office Action. For example, claim 1 as originally constituted required "configuring the FPGA for test including the FPGA forming an FPGA scan chain for simulating an external connection to an embedded device."

As explained in the present application, one problem addressed by the present invention is the testing of ASICs and other complex fixed logic circuits that are at least partially embedded within the FPGA. While the techniques of the present invention may be used to test a simple logic element, one particular embodiment includes an apparatus and corresponding method for testing a more complex fixed logic device. The Applicants do not believe that the cited art to Beebe and the other cited art disclose configuring the FPGA to facilitate it receiving a scan chain internally to test an embedded fixed logic device.

In reading the Official Action, however, the Applicant has determined that making the amendments made herein would be helpful for clarity but are not required

to overcome the cited art. Accordingly, the amendments are made to clarify the claimed invention and to more clearly define its novel and non-obvious aspects.

Accordingly, each rejected independent claim is amended to recite a fixed logic embedded device. Examples of such fixed logic embedded devices are not limited to but include ASICs, gaskets (fixed interfacing circuitry), etc. as is taught in the present application. The cited art does not teach or suggest fixed logic embedded devices as defined herein or an associated method of testing such fixed logic embedded devices. Further, as required by claim 1, the cited art does not suggest at least one device scan chain [that] is for testing the fixed logic embedded device and further wherein the at least one device scan chain is conducted into and through the FPGA to a scan chain logic circuit configured within the FPGA.

The cited art also does not teach forming a scan chain internal to the FPGA about a fixed logic embedded device within the FPGA as is required by claim 14. As may be seen, the art simply does not address a problem solved by the embodiments of the present invention, namely, how to test complex fixed logic circuitry embedded within an FPGA that is otherwise configurable.

As the references must teach or suggest all the claim limitation, i.e., a teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the cited references, and not based on applicant's disclosure. MPEP 2143, p. 2100-121 (August 2001). As the references do not satisfy this requirement for a proper rejection, it is believed that the claims as presently constituted are allowable over the art. Thus, the Applicants respectfully traverse this rejection and request reconsideration of the pending claims.

As each rejected independent claim is amended and arguments for allowability are made therefor, it is believed that the grounds of rejection that apply to the corresponding dependent claims are rendered moot and that the dependent claims are allowable for the same reasons. Because the rejected independent claims are amended, the Applicants will not address the grounds of rejection to an extent not already addressed above. Should the Examiner believe, however, that any of the grounds remain, he is invited to call the undersigned to request a phone conference to discuss the same to expedite the processing of this application.

Please direct any questions or comments to the undersigned attorney regarding the Notice of Allowance in this case.

## CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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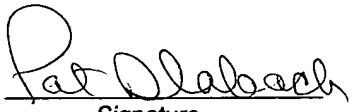
*I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 13, 2004.*

Pat Slaback
*Name*



*Signature*